Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.030”**

**.030”**

**T**

**A**

**C**

**BACKSIDE IS NOT CATHODE AND**

**MUST BE ELECTRICALLY ISOLATED.**

**(T = Metallization Test Pad)**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” min**

**Backside Potential: ISOLATED**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .030” X .030” DATE: 8/26/21**

**MFG: MSC / CDI THICKNESS .010” P/N: CD4572A / 1N4572A**

**DG 10.1.2**

#### Rev B, 7/1